A Cascaded Flying Capacitor Multilevel Inverter with Double-Boost Voltage Gain and reduced capacitor count for solar PV systems

Manxin Chen[1], *Student Member*, *IEEE*, Yat-Chi Fong[2], and Poh Chiang Loh[1]
[1]Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong
[2]Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong
E-mail: mxchen@link.cuhk.edu.hk[1]; yc-chi.fong@connect.polyu.hk[2]

***Abstract*—Fed by a mass of photovoltaic (PV) panels in series, the traditional buck-type flying-capacitor (FC) multilevel inverter has poor operational reliability in grid-connection application. In order to obtain a step-up output voltage, a novel five-level voltage source inverter is proposed by cascading two FC cells. The proposed inverter reduces the number of capacitors compared to the traditional buck-type topology with the same number of voltage levels. Moreover, the voltages of the capacitors can be self-balanced without using any other active-balancing strategies. Descriptions and theoretical analyses of the proposed inverter are given, followed by simulation results verifying its feasibility.**

Keywords—Power converter, switched-capacitor, flying-capacitor, multilevel inverter

I. Introduction

The ever-growing PV distributed generation has given birth to various power converters/inverters to couple the PV modules to the ac mains [1]. During this process, the leakage current induced by the parasitic capacitance between the PV arrays and the ground needs to be suppressed. And the use of multilevel inverters has been demonstrated as an appealing method [2]. Compared to the two-level VSI, the three-level VSI improves the quality of the output voltage with low total harmonic distortion (THD). Meanwhile, the voltage stresses on the power switches are reduced, which facilitates the utilization of low-voltage devices.

In general, the traditional MLIs can be divided into three groups including the diode-clamped or neutral-point-clamped (NPC) MLI, the capacitor-clamped or flying-capacitor (FC) MLIs, and the cascaded-full-bridge (CHB) MLIs. Among various multilevel inverter topologies, the FC multilevel inverter is regarded as a good candidate due to its inherent capacitor voltage balancing (Fig. 1(a)) [3]. However, FC multilevel inverter may use more capacitors, some of which are with voltages higher than the peak value of the ac output. Furthermore, the step-down feature is not suitable for the grid-connection application, since the output voltages of the PV panels are relatively low (mostly less than 100 V). Therefore, as a grid inverter, it needs to boost the source-voltage to the predefined grid voltages (110 V or 220 V rms) [4]–[6]. Otherwise, the input of the grid inverter requires a number of PV modules connected in series, which increases the burden of maximum power point tracking and reduces the operational reliability.

In this work, a novel five-level inverter is proposed by cascading two FC cells as shown in Fig. 1(b). The proposed inverter has the following features.

- The boosted output voltage is achieved with a voltage gain of two.
- The number of capacitors is reduced without using high voltage-rating capacitors.
- The voltages of the capacitors can be self-balanced.

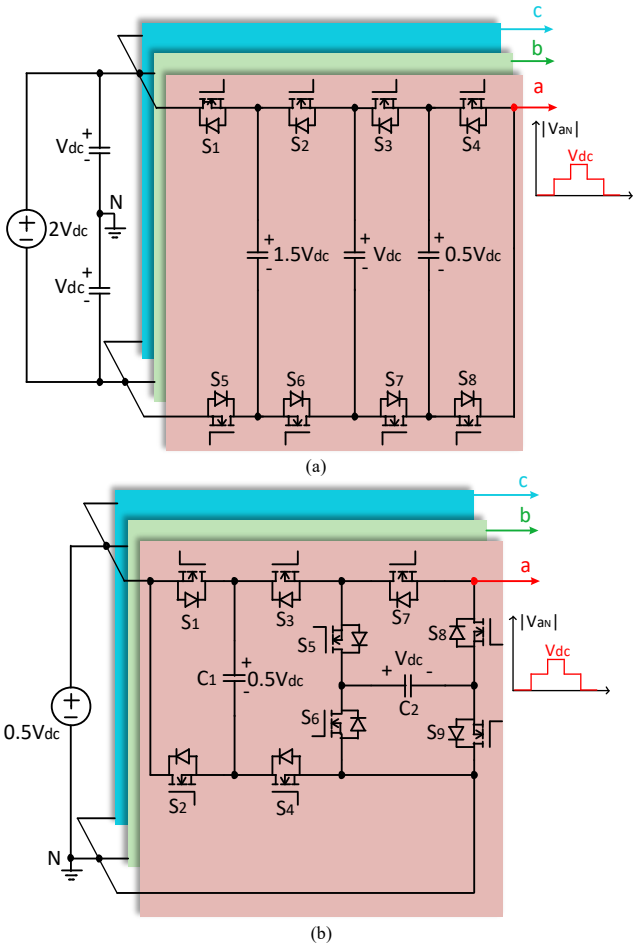

Fig. 1. Topologies of the (a) traditional FC buck-type five-level inverter [3] and (b) the proposed FC boost-type five-level inverter, both with maximum $V_{aN} = V_{dc}$.

For simplicity, only a single phase-leg is considered as shown in Fig. 2 and will be subsequently analyzed. As can be seen, the ac output and the DC input are commonly grounded which means the leakage current can be effectively suppressed for the PV systems.

II. Operating Mechanism Of The Proposed Inverter

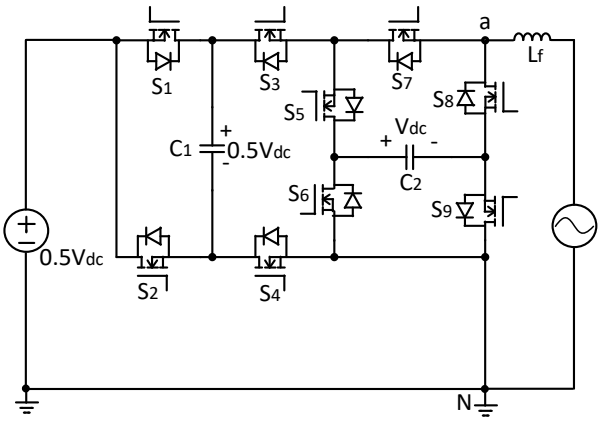

Fig. 2. Single-phase configuration of the proposed inverter.

The proposed five-level inverter has six operating states as depicted in Fig. 3. Although MOSFETs are used to represent the power switches, they can also be replaced by IGBTs, each anti-parallel connected with a diode. It should be mentioned that the proposed inverter can operate under any power factor, but for PV applications, the unity power factor is usually considered.

In State I (Fig. 3(a)), the switches S_2, S_3, S_5, S_7, and S_9 are turned on. The dc source in series connected with capacitor C_1 discharges to the capacitor C_2, which is supplying the ac output ($V_{aN} = V_{dc}$). In State II (Fig. 3(b)), the switches S_1, S_3, S_4, S_7, and S_9 are turned on. The dc source discharges to the capacitor C_1, which is feeding the ac output ($V_{aN} = 0.5V_{dc}$). In State III (Fig. 3(c)), the switches S_1, S_3, S_4, S_8, and S_9 are turned on. The dc source discharges to the capacitor C_1. The ac output is in the null (zero) state ($V_{aN} = 0$). In State IV (Fig. 3(d)), the switches S_2, S_3, S_5, S_8, and S_9 are turned on. The dc source in series connected with capacitor C_1 discharges to the capacitor C_2. The ac output is also in the null state. In State V (Fig. 3(e)), the switches S_1, S_3, S_5, and S_8 are turned on. The capacitor

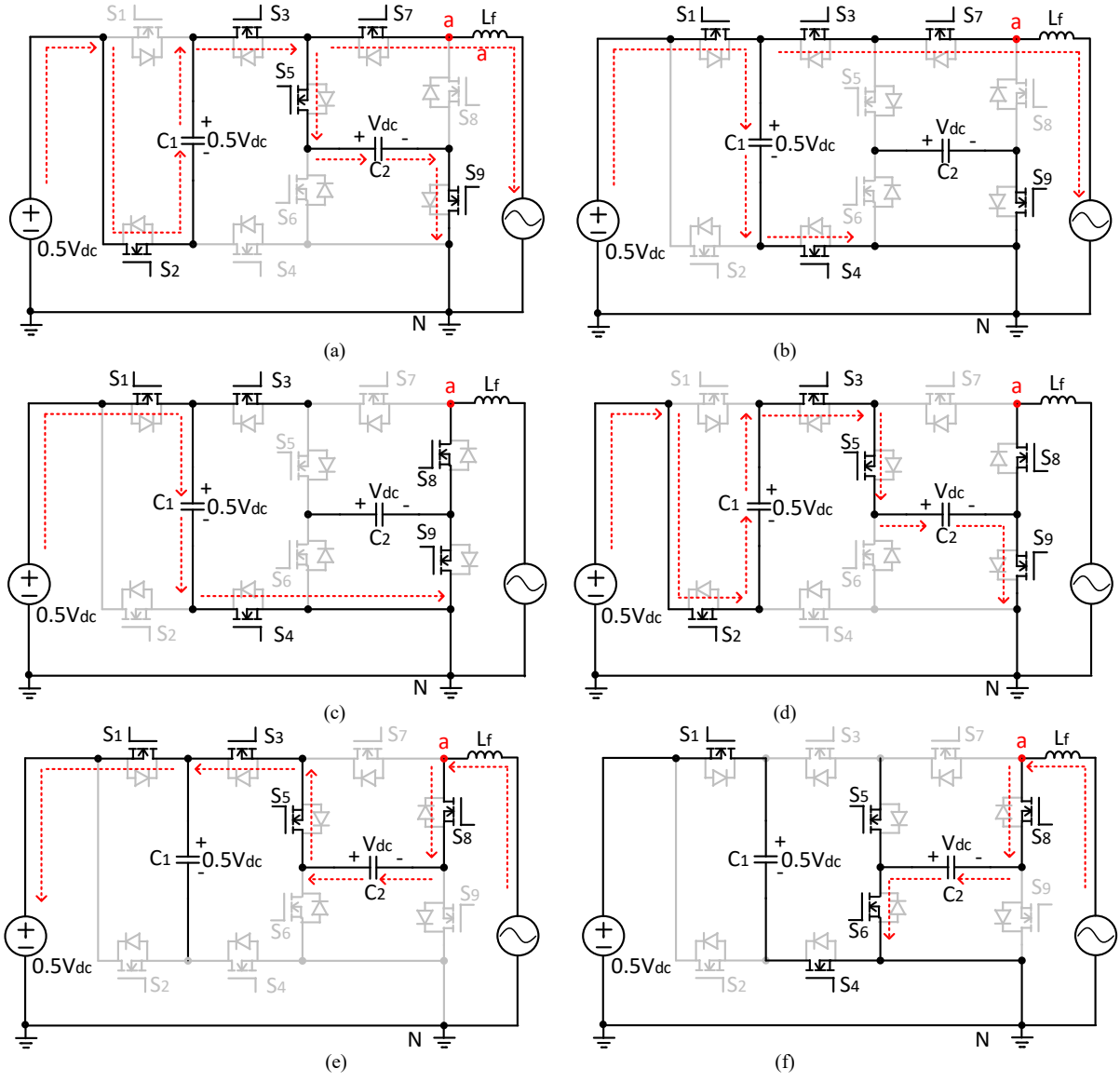

Fig. 3. Operating states with AC output voltage (a) $V_{aN} = V_{dc}$, (b) $V_{aN} = 0.5V_{dc}$, (c)-(d) $V_{aN} = 0$, (e) $V_{aN} = -0.5V_{dc}$, and (f) $V_{aN} = -V_{dc}$ (red dashed line represents the current flowing path).

TABLE I. OPERATING STATES OF THE CAPACITORS

	States	V_{aN}	C_1	V_{C1}	C_2	V_{C2}
A_1	I	V_{dc}	Dis.	↓	Ch.	↑
	1↓ 1↓	1↓				
	II	$0.5V_{dc}$	Ch.	↑	X	—
A_2	II	$0.5V_{dc}$	Ch.	↑	X	—
	1↓ 1↓	1↓				
	III/IV	0	Ch. or Dis.	↑ or ↓	X or Ch.	— or ↑
A_3	III/IV	0	Ch. or Dis.	↑ or ↓	X or Ch.	— or ↑
	1↓ 1↓	1↓				
	V	$-0.5V_{dc}$	X	—	Dis.	↓
A_4	V	$-0.5V_{dc}$	X	—	Dis.	↓
	1↓ 1↓	1↓				
	VI	$-V_{dc}$	Ch.	↑	Dis.	↓

C_2 anti-series connected with dc source discharges to the output ($V_{aN} = -0.5V_{dc}$). In State VI (Fig. 3(f)), the switches S_1, S_4, S_5, S_6, and S_8 are turned on. The capacitor C_2 discharges to the output ($V_{aN} = -0.5V_{dc}$).

Multicarrier modulation (Fig. 4) can be used to generate the above six states for the proposed inverter. There are only two operating states in each carrier band. For example, when carrier A_1 is enforced, operation only includes states I-II, with output voltage transiting between V_{dc} and $0.5V_{dc}$, respectively.

In each carrier band (A1-A4), the capacitors may be charged (Ch.), discharged (Dis.) or in idle (X) state. Accordingly, the capacitor voltages may increase (↑), decrease (↓), or keep constant (—) as shown in Table I.

III. THEORETICAL ANALYSIS

The voltage gain of the proposed inverter can be expressed as

$$G = \frac{V_{aN\_max}}{V_{in}} = \frac{V_{dc}}{0.5V_{dc}} = 2 \quad (1)$$

where V_{aN_max} is the maximum output voltage and V_{in} is the dc input source-voltage.

From Fig. 3(a)-(f), the voltages across the power switches when they are off can be found and their relationships are expressed as

$$V_{ds1} = V_{ds2} = V_{ds3} = V_{ds4} = V_{ds5} = 0.5V_{dc} \quad (2)$$

$$V_{ds6} = V_{ds7} = V_{ds8} = V_{ds9} = V_{dc} \quad (3)$$

It can be seen that the voltage stresses (blocking voltage) of the power switches are V_{aN_max} or $0.5V_{aN\_max}$. Moreover, the voltages across the capacitors C_1 and C_2 are $0.5V_{aN\_max}$ and V_{aN_max}, respectively, which means lower voltage rating capacitors can be selected compared to the traditional FC buck-type inverter (Fig. 1 (a)).

Table I also shows that both V_{C1} and V_{C2} can be self-balanced, since two or more charging states for the

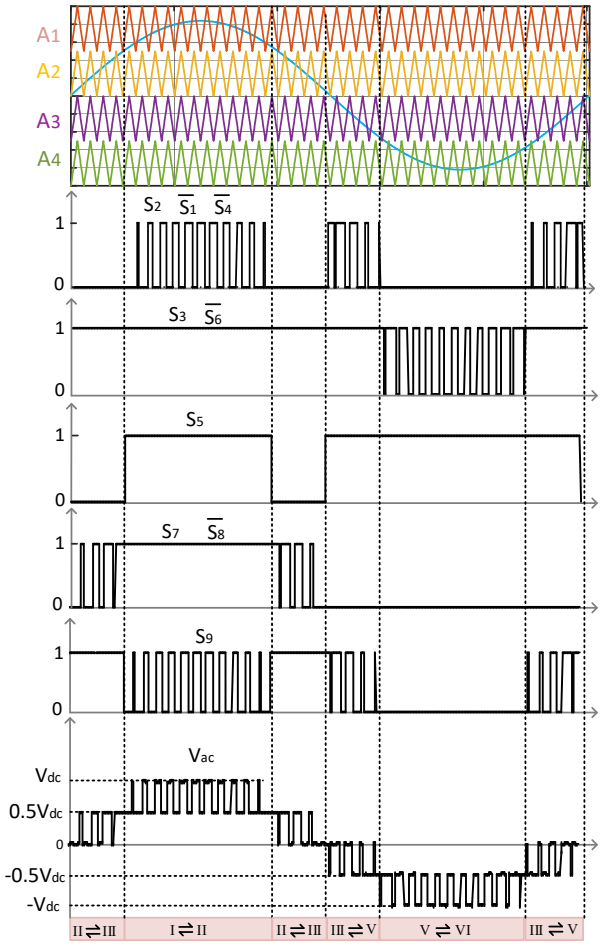

Fig. 4. Multicarrier modulation strategy (state III is selected to generate $V_{aN} = 0$ here).

capacitors can be found. However, one can find that the voltage V_{C2} consistently drops during carrier band A_4, because it discharges to the output in states V-VI. Therefore, C_2 should have relatively large capacitance to hold the capacitor voltage V_{C2}. Assume that the voltage ripple (ΔV_{C2}) is less than $1\%V_{aN\_max}$, the following equation can be written

$$\frac{\Delta V_{C2}}{V_{a\_max}} = \frac{1}{V_{a\_max}C_2}\int_{t_1}^{t_2} i_o(t)$$

which can be rewritten as

$$\frac{M_{ac}}{C_2 R}\int_{t_1}^{t_2} sin(\omega t) \le \frac{1}{100} \quad (4)$$

where $i_o(t)$ is the ac output current and also the capacitor-discharge current of C_2 during States V-VI; R is the load resistance and M_{ac} is the modulation index of the sinusoidal reference ($M_{ac} > 0.5$).

By letting $M_{ac}\sin(\omega t) = 0.5$, the time t_1 can be found by

$$t_1 = \frac{1}{\omega} sin^{-1}\left(\frac{0.5}{M_{ac}}\right) \quad (5)$$

where ω is the angle frequency of the ac output. For t_2, it can be calculated according to periodicity

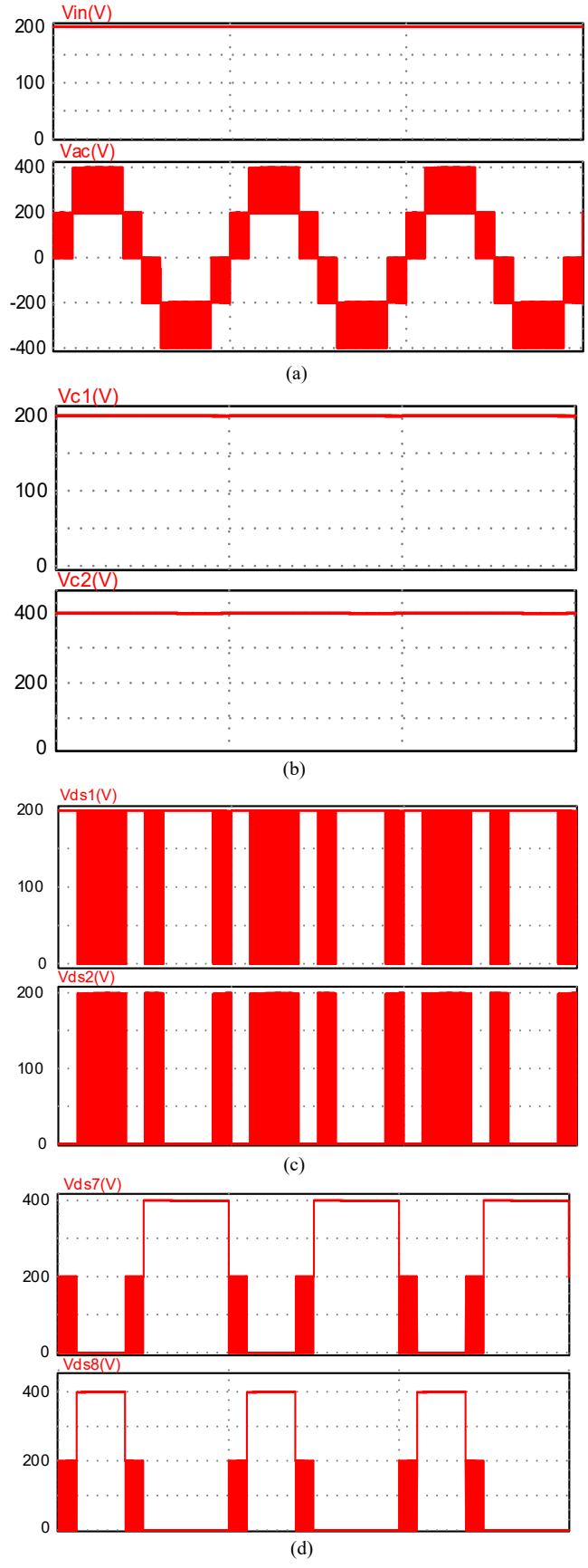

Fig. 5. Key voltages of simulation results including (a) V_{aN}, V_{in}; (b) V_{C1}, V_{C2}; (c) V_{ds1},V_{ds2}; (d) V_{ds7}, V_{ds8}.

$$t_2 = \frac{\pi}{\omega} - t_1 \tag{6}$$

Using (4)-(6), the capacitance of C_2 can be found as

$$C_2 \geq \frac{100M_{ac}[\cos(\omega t_2) - \cos(\omega t_1)]}{R\omega} \tag{7}$$

The equation in (7) suggests that the capacitor size would be inversely proportional to the fundamental output frequency and loading resistance.

IV. Simulation Results

The proposed inverter has been simulated with the following parameters, and the simulation results are shown in Fig. 5 (a)-(d). The input voltage ($\boldsymbol{V_{in}}$) was $\boldsymbol{200\,V}$ ($\boldsymbol{V_{dc}} = \boldsymbol{400\,V}$), and the nominal output power was $\boldsymbol{1\,kW}$. Switching frequency for the power switches was set to $\boldsymbol{f_s = 50\,kHz}$. The selected capacitances were $\boldsymbol{C_1 = 200\,\mu F}$ and $\boldsymbol{C_2 = 4000\,\mu F}$, respectively. Simulation results show that two times of voltage gain is achieved. A five-level ac output with a maximum voltage of 400 V (Fig. 5(a)) was generated. The capacitor voltages, V_{C1} and V_{C2} are depicted in Fig. 5 (b). With the aforementioned parameters, the voltage across the capacitors were self-balanced to stable values of approximately $0.5V_{dc}$ and V_{dc}. The blocking voltages for some of the switches $\boldsymbol{S_1}$- $\boldsymbol{S_2}$ and $\boldsymbol{S_7}$- $\boldsymbol{S_8}$ are shown in Fig. 5 (c)-(d). Their values were $0.5V_{dc}$ and V_{dc}, which match the calculations in (2)-(3).

V. Conclusion

A novel five-level voltage source inverter is proposed by cascading two FC cells. Twofold voltage gain is achieved by only using two capacitors, whose voltage-ratings are relatively low. Furthermore, the voltages of the capacitors can be self-balanced, which means no active-balancing circuits are required. Some simulated results initially verify its feasibility in this digest. More details are to be presented in the final paper. It is expected that the proposed multilevel inverter is suitable for renewable energy applications where boosted ac voltages are required.

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